

## Wafer Bumping

### Wafer Bumping Processes and Die Level Interconnect Technology Services



The electrical and mechanical connection between a die and substrate is one of the most critical elements of any flip chip package structure. Predominantly lead-tin and lead-free solders at the present time, these connections – or bumps –

must exhibit superior adhesion to the die, minimal resistance, and result in high assembly yields. Solder bumps are formed by using either thin film metal deposition, plating or ball loading techniques.

Amkor offers state-of-the-art capability in electroplated solder technologies in multiple strategic locations (Korea, China and Taiwan). These locations are uniquely situated adjacent to major foundry sources to enable our customers reduced time-to-market with integrated factory logistics.

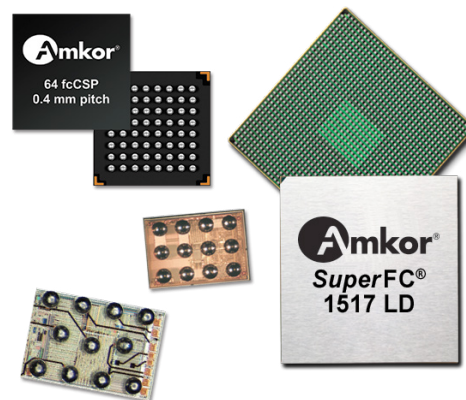
Our Taiwan facility is a world-class solder bumping line with HVM production capability for 200 mm and 300 mm wafers. Eutectic, lead-free and Cu pillar solder compositions (all low alpha) are production certified. In addition, the facility offers repassivation, single- and multi-layer redistribution processes for both flip chip and wafer level chip scale package applications.

Our Korea, China and Taiwan bumping operations are co-located with wafer probe, assembly and final test, enabling Amkor to provide complete "Turnkey" flip chip and WLCSP solutions in these key geographic locations. These facilities offer economy of scale as WLCSP continues to grow in the future. This combination of technology and manufacturing capabilities is unparalleled in the subcontract manufacturing industry.

### Bumping Process Specifics

Amkor's bumping process is production certified through the full package size range from WLCSP up through large die Flip Chip BGA.

<b>Wafer Size</b>	200 mm, 300 mm
<b>Solder Compositions</b>	63Sn/37Pb, 98.2Sn/1.8Ag (all available as low alpha: < 0.002 cts/hr/cm <sup>2</sup> ), SnAgCu, Doped alloys
<b>Pad Pitch Lower Limit</b>	50 μm
<b>Typical Production Bump Height</b>	150 μm array: 70 μm 125 μm peripheral: 75 μm
<b>Repassivation Coatings</b>	Polyimide, PBO, Low cure polymers
<b>Redistribution Materials</b>	Copper

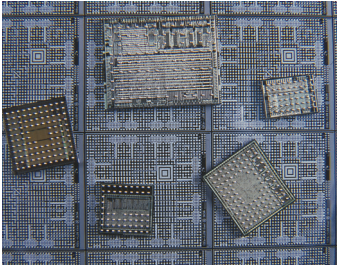


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### Related Processes/Services



Wafer Bumping and Wafer Level Chip Scale Packaging (WLCSP) use many of the same basic process steps in production. Key WLCSP developments have resulted in improved wafer level technology known as CSPnl. CSPnl combines plated copper technology and advanced

photopolymers to produce the industry's most robust wafer level solutions. CSPnl is available down to 0.3 mm pitch and supports a range of solder volumes to meet customer requirements.

Closely related to both bumping and WLP production is "die processing" capability, which consists of process steps that transform either bumped or WLCSP product from wafer form into die form. Die processing typically involves test, singulation, inspection and pick-and-place, and Amkor offers these full turnkey services to support our customers at multiple facilities around the world.



### Technology Development

Amkor maintains strong initiatives in the area of technology development to further support customers' future needs. Continuous improvement programs are in place to optimize and cost-reduce the wafer bumping processes.

- Electroplating capabilities will support fine pitch bumping and copper pillar structures
- Higher performance passivation materials
- WLCSP die size support to greater than 144 I/Os and 0.3 mm pitch



Amkor's technology leadership continues to advance flip chip technology as part of our broad portfolio of over 1000 packages. We will continue to partner with leading companies to bring new flip chip products quickly to market. We have the vision and breadth to move flip chip interconnect off the drawing board and into production across a wide range of package formats.

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