Via² - Laser Embedded Conductor Technology

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ABSTRACT

While semiconductor technology progresses at an alarming rate, typically doubling in functionality every couple of years, the substrate portion of the integrated circuit (I.C.) packaging industry continues to fall further and further behind. This has created a significant technology gap, forcing the semiconductor manufacturers to compensate their chip design by adding more redistribution layers or even worse, adding additional size to the chip itself. There is, therefore, a real need for significant change in manufacturing methods used at the substrate level, to remove this ever widening gap and thus allow the chip manufacturers to continue their path towards reduction in size and cost, while still increasing product functionality.

A collaborative effort between Amkor Technology, Unimicron and Atotech, has led to a significant new breakthrough in substrate manufacturing techniques, allowing layer, design feature and format reduction (thus cost reduction) versus current state of the art technologies. This innovative method utilizes laser ablation techniques, together with specially developed plating processes, to form electrical paths for signal propagation embedded within the dielectric, rather than the more conventional conductors on the dielectric layer.

This paper is the second part of a two part paper co-authored by Atotech (Dave Baron) and Amkor Technology. This paper describes the opportunity to reduce the number of vias and layers in the substrate, the unique opportunity to optimize electrical performance, and the potential miniaturization in design as a result. A close look at this technology reveals the clear benefits and opportunity for significant gap closure required by the chip packaging industry today.

ELECTRICAL PERFORMANCE AND RELIABILITY DATA

Tables 1, 2 and 3 show the data from a few of the designs converted to the laser format to date, each listing both the original and the converted design data. Each original design listed in the tables is currently running in high volume production today. The data clearly demonstrates the benefit of the laser embedded circuits with the resultant reduction in both PTH and blind vias resulting. It is important to note that the conversion was only made possible by combining the embedded technology with electrical redesign for both power management and signal integrity.

Flip Chip Device	Original	Embedded
Total Layers	2-2-2	1-2-1
Total Thick /Core	1.05 / 0.8mm	1.00 / 0.8mm
Line / Space B.U.	30µ / 30µm	30µ / 30µm
Line / Space Core	75µ / 75µm	17µ / 18µm
Total # PTH	792	673
Total # Blind Vias	5324	1393
Package Level Reliability 37mm, 1315 I/O, 10x9mm Die, 1.0mm BGA & 200u Bump Pitch		Passed L3 260C, TCB 1000 cycles

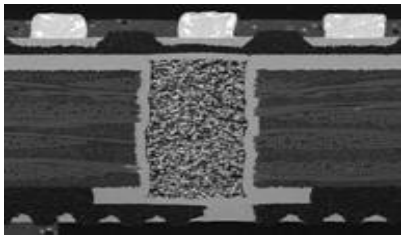

Table and Figure 1 – Substrate with laser formed circuits.

Flip Chip Device	Original	Embedded
Total Layers	2-2-2	1-2-1
Total Thick /Core	1.05 / 0.8mm	0.60 / 0.4mm
Line / Space B.U.	20µ / 25µm	20µ / 25µm
Line / Space Core	75µ / 75µm	12µ / 14µm
Total # PTH	981	614
Total # Blind Vias	9754	2683
Package Level Reliability 31mm, 899 I/O, 12x14mm Die, 1.0mm BGA & 200u Bump Pitch		Passed L3 260C, TCB 2000 cycles

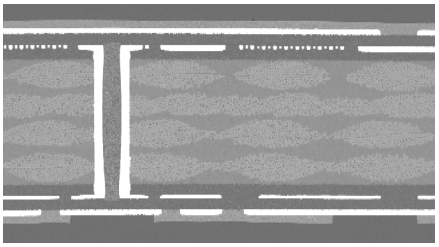

Table and Figure 2 – Substrate with laser formed circuits.

Flip Chip Device	Original	Embedded
Total Layers	2-2-2	1-2-1
Total Thick /Core	1.05 / 0.8mm	0.60 / 0.4mm
Line / Space B.U.	25 / 25µm	25 / 25µm
Line / Space Core	Not possible	10 / 12µm
Total # Blind Vias	5283	2376
Total # PTH	508	628
Package Level Reliability 20x25mm, 655 I/O, 8x8mm Die, 0.8mm BGA & 210u Bump Pitch		On-going L3 260C, TCB 100 cycles

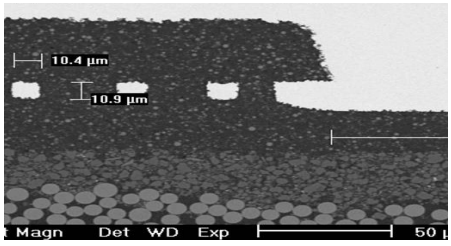

Table and Figure 3 – Substrate with laser formed circuits.

ELECTRICAL BENEFITS OF LASER EMBEDDED CIRCUITRY

The electrical and structural demands of 65nm silicon nodes and below will require extreme care in the design of all future substrates. This includes the choice of dielectric material in terms of mechanical and electrical performance. Material suppliers continue to produce lower loss and lower coefficient of thermal expansion materials to assist in this endeavor. However, in high speed applications, the length of interconnect from the die pad to the I/O is probably more important than the dielectric used in the substrate. Traditional substrates require many planes to manage both the power and electrical signal integrity. This only exacerbates the problem of length of interconnect. Inductance is increased as a result and the number of vias to interconnect the layers is multiplied.

With the reduction in the number of layers, shortened signal paths and "guarded signal" offered by the embedded circuit techniques, electrical performance is no longer compromised, but instead enhanced. Figure 4 demonstrates the coplanar coupling provided with the laser embedded circuit. In this case, the impedance can be tuned to less than 10% variance.

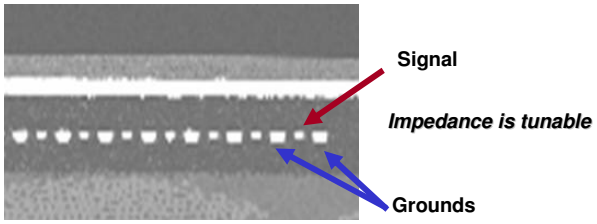

Figure 4 – Coplanar ground embedded circuits.

Figures 5 and 6 demonstrate the electrical field generated by the copper circuits. Figure 5 shows the standard electrical field with a resonating signal to either above or below the signal layer, and in sometimes to both. However, only 70% of the electrical field resonates above or below the circuit while 30% of the electrical field resides within the circuitry itself. This induces both noise and poorer impedance control. The problem of managing impedance in this manner continues as the dielectric thickness varies along the length of the net and thus the impedance with it.

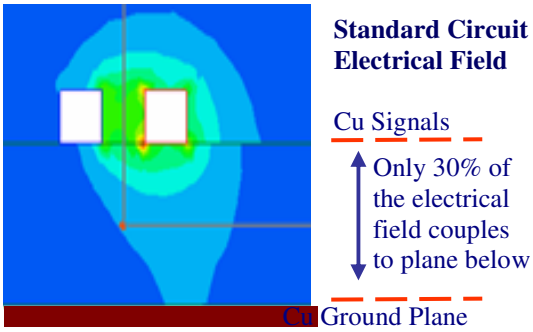

Figure 5 – Electrical field and typical ground plane below.

Figure 6 shows the electrical field created by a laser embedded circuit. The electrical field can be nearly fully captured by extending the biased signals (grounds) to a lower depth than the active signals. Since the distance to ground is managed by the laser resolution and registrational accuracy of the laser, the impedance is well controlled to less than 10% variance.

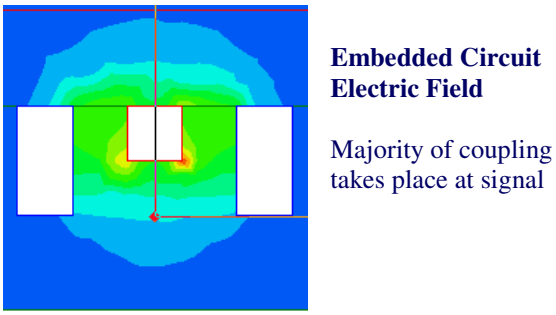

Figure 6 – Embedded circuit and electrical field.

The structural impact of the guarded signal clearly provides a better coupling mechanism for signal integrity as compared to traditional approaches to impedance management today, demonstrated in Figure 5 and 6. The relationship of dielectric thickness to trace signal width is the key method of impedance management in traditional substrates while with the embedded approach, a within plane technique is used instead to eliminate the dependence on dielectric thickness control across the length of the net. The laser embedded approach eliminates one key variable to manage in the dielectric thickness variance.

By lengthening the biased grounds, the signal integrity can be improved by capturing much of the electrical field provided by the active signal and preventing transmission to nearby active signals that would traditionally be left

unprotected. The biased signals (grounds) act as guards to not only improve the impedance control but to also reduce the noise generated in standard circuits today. Figure 7 demonstrates the signal integrity improvement offered by the guards, showing a 2x improvement in noise reduction by using this concept. In this example, the biased signals were extended to 1.5x the depth of the active signal.

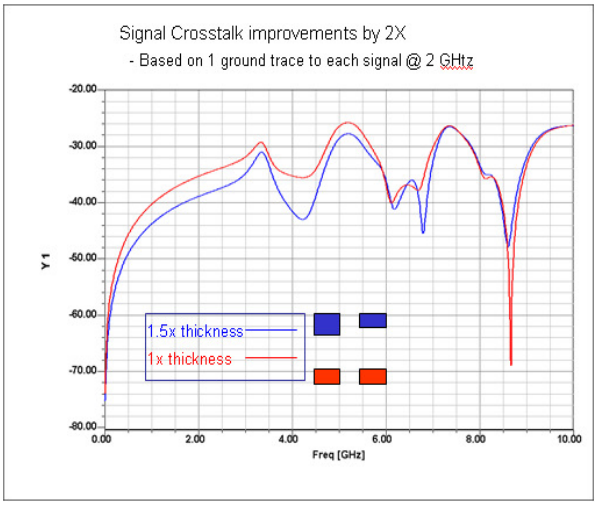

Figure 7 – Embedded circuit and cross talk

Power management is critically important in advanced semiconductor node devices (less than 65nm). Figure 8 demonstrates how the power integrity is managed in the laser embedded circuits. A novel approach is used to control the noise that can be generated by traditional circuits today. Figure 8 shows a standard 2-2-2 substrate used in the graphics processor business today in high volume. A reduction of this device into the laser embedded circuitry (1-2-1) without power management shows a noisier device as a result of the layer pair reduction. However, a utilizing the power management techniques, the device is pulled back to within budget on the noise control.

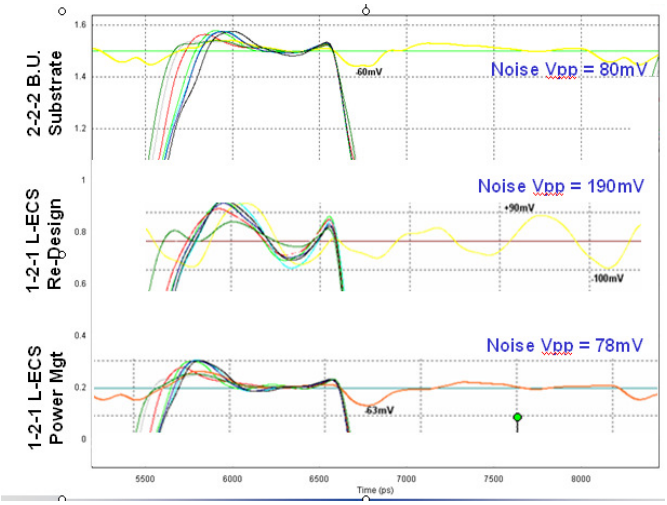

Figure 8 – Embedded circuit and power management.

An additional benefit of the laser embedded circuit is the surface profile. The surface profile of the copper trace also has an affect on the signal integrity of the circuit. At higher speeds the signal travels more along the surface of the copper trace rather than in the bulk metal itself. This requires as smooth a surface interface as possible on the copper circuit. This is counter intuitive to the requirements of copper circuits today as they require a profile on the circuit to allow subsequent adhesion to the next layer dielectric. Today, to assure a high process yield and a reliable product under stress, a degree of copper surface roughness is created, typically at or near 2µm. Since the circuit pattern formation happens within the dielectric, rather than on the surface of the dielectric with the laser embedded approach, this concern is alleviated.

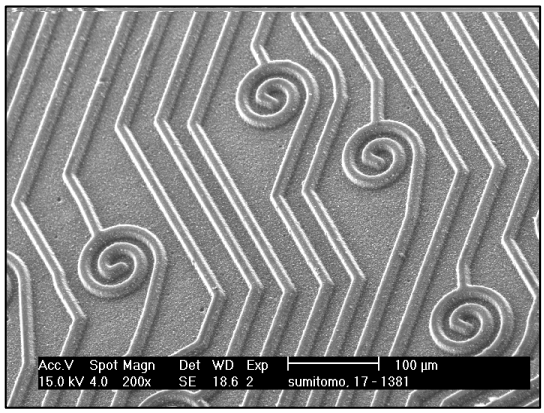

Figure 9 – Embedded circuit with inductors [1].

Another unique benefit of this technology is the ability to create unique features and/or shapes such as that shown above in Figure 9. Figure 9 shows the pattern created using a reverse mask with excimer ablation, showing dielectric removed outside of the key features in this case rather than the typical process of removing dielectric where the features will be formed only. Due to the size of the features created transmission delays can easily be created within small spaces rather than trying to route the signal between via pads and other key nets within the device. Other unique features such as capacitors and resistors are being contemplated using the embedded approach as well, making use of the ability to produce both extremely small features and features at varying depths.

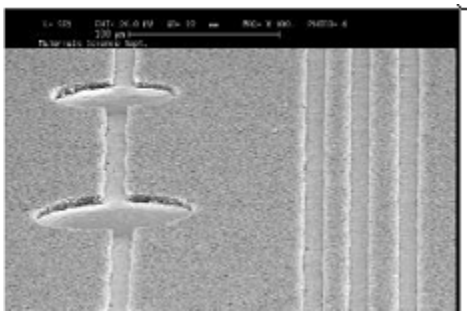

Figure 10 – Finished embedded circuits and via lands [2].

CONCLUSION AND CHALLENGES OF ADVANCING SILICON NODES

Looking to the future, the key issues for substrates and the substrate suppliers for next generation devices will be signal integrity and latency, which will need to be optimized through minimized matched pair routing distances from die to motherboard, surface planarity, cost and reliability [3]. As the signal and power integrity become increasingly important in 65nm and below silicon node devices, the impedance control, loop inductance and cross talk take on greater importance. Impedance requirements will be allowed to vary less than 10% overall, loop inductance will drop to less than 3pH and cross talk allowance will drop to under 80mV. All three issues are addressed well with the embedded approaches discussed in this paper and again demonstrated in Figures 11 and 12. By using guard traces to shield against noise with signals in close proximity, both the noise and impedance control can be managed to meet all electrical requirements today and for the foreseeable future.

REFERENCES

[1] Jain, K., et al., (2002). "Large-Area Excimer Laser Lithography and Photo ablation Systems", Microlithography World, Vol. 11, No. 3, p. 8, Aug. 2002.

[2] Baron, et al. (2006). "Unveiling the Next Generation in Substrate Technology", Pan Pacific Technology Symposium, January 2007.

[3] BPA Consulting (2006), "Worldwide High-Speed Electronics Technology and Market Trends for the Years 2006-2016," Executive Market and Technology Forum, pp. 59, 64-65, Sept. 2006.