Data Sheet

Flip Chip CSP Packages (fcCSP)

Amkor Technology offers the Flip Chip CSP (fcCSP) package – a flip chip solution in a CSP package format. This package construction utilizes Pb-Free (or Eut. SnPb) flip chip interconnect technology, in either area array or peripheral bump layout, replacing standard wirebond interconnect. The advantages of flip chip interconnect are multiple: it provides enhanced electrical performance over standard wirebond technology, it allows for a smaller form factor due to increased routing density, and the elimination of wire-bond loops. Current wafer bump technology and flip chip assembly process allows for peripheral flip chip bumping or area array bumping, with either solder or Cu pillar bump technology.

The fcCSP is based on Amkor's proprietary ChipArray® BGA (CABGA) package construction, using cutting edge thin core laminate substrates. The package is assembled in strip format, in either bare die or overmolded format, and saw singulated for manufacturing efficiency and cost minimization. Pattern plating for fine line/spaces, via-in-pad substrate structure, and thin core substrate panel processing allow for increased routing density and enhanced electrical performance, making fcCSP an attractive option for advanced CSP applications where electrical performance is a critical factor.

The fcCSP is available in both thin core laminate substrate technology as well as build up (for further enhanced routing). Package size ranges from 2 mm to 17 mm, accommodating BGA ball pitches from 0.4 mm to 1.0 mm. In addition to BGA technology, the fcCSP is also available in LGA format, allowing for a lower minimum package thickness.

Features

- Can design to high frequency applications of 60+ GHZ
- 9-1500+ ball counts
- Target market – cell phones, handheld electronics, applications where high density packaging is required, multi-die and/or designs with passive components
- Array strip production
- Thin core laminate or buildup substrate construction
- Bare die with underfill, overmolded, molded underfill and exposed die molded versions available
- Accommodates package sizes from 2 mm to 17 mm
- Flip chip bump pitches of 80 µm peripheral and 130 µm area array

fcCSP

- Cu pillar flip chip interconnect for fine bond pitches down to 30 µm/60 µm staggered
- Available in 0.4-1.0 mm BGA ball pitch, as well as LGA interconnect
- Minimum package thickness of < 0.4 mm for LGA interconnect, < 0.6 mm for 0.4 mm and 0.5 mm BGA pitch
- Turnkey Solution – design, bumping, bumped wafer probe, backgrind, assembly, test
- Much better signal to noise ratio at higher frequencies (>1 GHz) versus wirebonded packages
- Low inductance of flip chip bumps – short, direct signal path
- Flexible customizable substrate routing. Smaller possible body size than wirebond CSP due to additional space not required for wirebond pads

Applications

The fcCSP package is an attractive option for handheld/portable electronics where, in addition to performance, package size is critical. Some applications which have adopted fcCSP are high-performance workstations, servers, data communication products and some emerging applications such as netbooks and RF applications where electrical performance is critical. The elimination of wirebond loops allows for a low inductance connection to the die while the increased routing density enables optimized electrical paths for critical high frequency signal lines.

Thermal Performance

Theta JA (°CW)

- 12 x 12 mm, 441 lead package with 7.5 mm x 7.5 mm die, 0.5 mm pitch, 0.45 mm mold cap
- 0 LFPM, 4 layer PC board
- Junction ambient thermal resistance = 21.3°C/W

Electrical Performance

8 x 8 mm body, 176 lead, 0.5 mm ball pitch, simulated results @ at 100 MHz

	Min	Max
Inductance	0.34 nH	2.15 nH
Capacitance	0.19 pF	0.64 pF
Resistance	22 mΩ	84 mΩ

Reliability Qualification

Package Level:

• Laminate Moisture Sensitivity	JEDEC Level 3 @ 260°C 30°C/60% RH, 192 hours
• Ceramic Moisture Sensitivity	JEDEC Level 1 @ 260°C 85°C/85% RH, 168 hours
• PCT	121°C/100% RH, 96 hours
• Temp/Humidity	85°C/85% RH, 1000 hours
• Temp Cycle	-55°C/+125°C, 1000 cycles
• High Temp Storage	150°C, 1000 hours

Board Level:

8 mm body, 64 lead, 0.33 mm PWB NSMD pad size

• Thermal Cycle	-40°C/+125°C, 1 cycle/hour, 3000 cycles
• Thermal Cycle	-40°C/+125°C, 2 cycles/hour, 2500 cycles

17 mm body, 1019 lead

• Thermal Cycle	0°C/+100°C, 1 cycle/hour, 2230 cycles

Visit Amkor Technology online for locations and to view the most current product information.

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Process Highlights

- Die size: 0.5 mm to 13 mm
- Package size: 2 mm to 17 mm
- Bump pitch (LF or Eutectic)
  - In-line: 80 µm
  - Array: 130 µm
- Bump pitch (Cu pillar)
  - In-line: 30/60 µm staggered
  - Array: 130 µm

Standard Materials

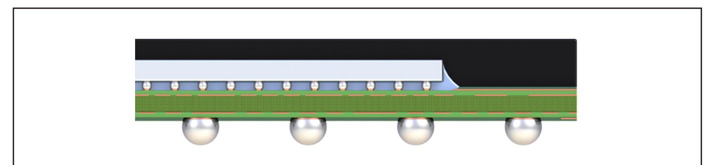
- Package substrate:
  - NXA, NS, NS-LC, NSF-LCA
  - E679: FG, FGB, FGBS, GT
  - E700G, E705G
  - DS7409HG, DS7409HGB(S), DS7409HGB(LE)
  - ELC4785GSB, ELC4785THB, ELC4785THG
- Bump: Pb-Free, Eutectic, Cu pillar
- Encapsulant: Epoxy mold compound
- Solder balls: Lead free, Eutectic, Pb-Free

Test Services

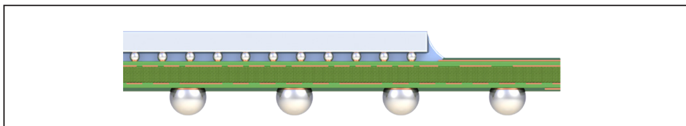
- Program generation/conversion
- Product engineering
- Wafer sort
- -55°C to +165°C test available
- Burn-in capabilities
- Tape and reel services

Shipping

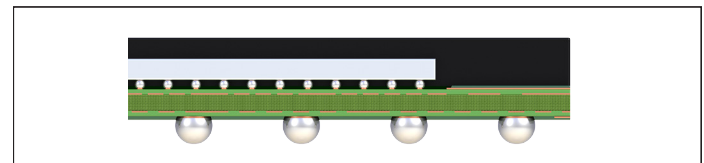
- JEDEC trays



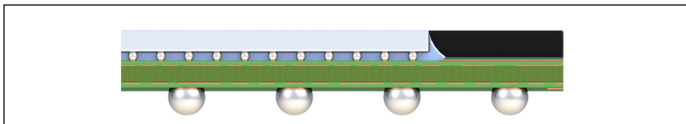
Overmolded, Capillary Underfill



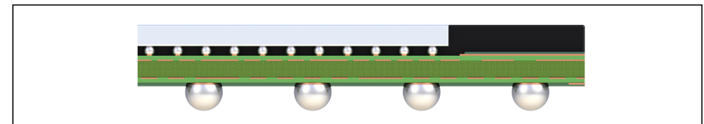
Bare Die, Capillary Underfill



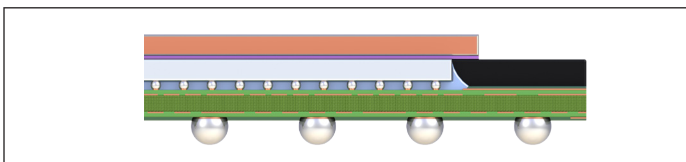
Overmolded, Molded Underfill



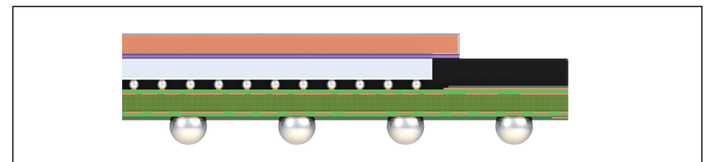
Exposed Die Molded, Capillary Underfill



Exposed Die, Molded Underfill



Exposed Die Molded, Capillary Underfill Plate Heatsink



Exposed Die Molded, Molded Underfill Plate Heatsink

fcCSP

Configuration Options

fcCSP Package Dimensions (mm)

Pkg X	Pkg Y	# BGAs	Ball Dia.	BGA Pitch
06.5	08.5	52	0.300	0.50
06.0	05.0	102	0.250	0.45
06.0	06.0	90	0.300	0.50
06.0	06.0	137	0.200	0.40
06.5	06.5	97	0.250	0.40
06.5	06.5	225	0.250	0.40
06.5	06.5	225	0.250	0.40
07.0	07.0	64	0.450	0.80
07.0	07.0	88	0.300	0.50
07.0	07.0	88	0.300	0.50
07.0	07.0	132	0.300	0.50
07.0	07.0	191	0.250	0.40
07.0	07.0	208	0.250	0.40
07.0	07.0	287	0.250	0.40
07.0	07.0	287	0.250	0.40
09.0	09.0	192	0.300	0.50
09.0	09.0	196	0.300	0.50
09.0	09.0	383	0.250	0.40
09.0	09.0	383	0.250	0.40
09.0	09.0	383	0.250	0.40
09.5	09.0	330	0.250	0.40
09.5	09.0	330	0.200	0.40
10.0	10.0	144	0.460	0.80
10.0	10.0	144	0.400	0.80
10.0	10.0	108	0.400	0.80
10.0	10.0	249	0.250	0.525/0.67
10.0	10.0	249	0.250	0.53
10.0	10.0	384	0.250	0.40
10.0	10.0	424	0.250	0.40
10.0	10.0	454	0.250	0.40
11.0	08.0	300	0.250	0.40
11.0	11.0	301	0.300	0.50
11.0	11.0	456	0.250	0.40
11.0	11.0	576	0.250	0.40
11.0	11.0	576	0.250	0.40
11.0	11.0	576	0.250	0.40
12.0	12.0	121	0.600	1.00
12.0	12.0	168	0.250	0.50
12.0	12.0	216	0.250	0.40
12.0	12.0	216	0.250	0.40
12.0	12.0	409	0.250	0.40
12.0	12.0	441	0.300	0.50
12.0	12.0	441	0.300	0.50

Pkg X	Pkg Y	# BGAs	Ball Dia.	BGA Pitch
12.0	12.0	512	0.250	0.40
12.0	12.0	512	0.250	0.40
12.0	12.0	515	0.250	0.50
12.0	12.0	524	0.250	0.40
12.0	12.0	547	0.250	0.40
12.0	12.0	547	0.250	0.40
12.0	12.0	560	0.250	0.40
12.0	12.0	560	0.250	0.40
12.0	12.0	560	0.250	0.40
12.0	12.0	560	0.250	0.40
12.0	12.0	569	0.250	0.40
12.0	12.0	580	0.250	0.40
12.0	12.0	617	0.250	0.40
12.0	12.0	617	0.200	0.40
12.0	12.0	697	0.250	0.40
12.0	12.0	700	0.200	0.40
12.0	12.0	714	0.250	0.40
13.0	13.0	225	0.460	0.80
14.0	14.0	220	0.325	0.50
14.0	14.0	240	0.250	0.50
14.0	14.0	240	0.225	0.50
14.0	14.0	240	0.225	0.50
14.0	14.0	256	0.250	0.40
14.0	14.0	256	0.250	0.40
14.0	14.0	256	0.250	0.40
14.0	14.0	256	0.250	0.40
14.0	14.0	289	0.460	0.80
14.0	14.0	289	0.460	0.80
14.0	14.0	617	0.300	0.50
14.0	14.0	676	0.250	0.50
14.0	14.0	681	0.250	0.5/0.707
14.0	14.0	756	0.250	0.40
14.0	14.0	789	0.250	0.40
14.0	14.0	976	0.250	0.40
14.0	14.0	976	0.200	0.40
14.0	14.0	980	0.250	0.40
15.0	15.0	216	0.325	0.50
15.0	15.0	216	0.300	0.50
15.0	15.0	249	0.300	0.80
15.0	15.0	324	0.500	0.80
15.0	15.0	841	0.200	0.50

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