Flip Chip Packaging of Low-k Devices

Low-k has become a hot topic as most 90nm devices and all 65nm devices utilize low-k dielectric. By most definitions, an insulating layer must have a dielectric constant of < 3.0 to qualify as "low-k". The lower the dielectric constant, the lower the capacitance which is particularly important as dielectric layers become thinner; however, to lower the dielectric constant significantly below ~2.7, porosity (air pockets) is increased which makes the layer more brittle and reduces strength so most fabs have settled on dielectric materials with a K value of ~2.8-2.9 at 90nm with decreasing values at 65nm.

Amkor works closely with the world's largest foundry's and has qualified common industry low-k dielectric materials up to 23mm die size. Amkor has developed specific assembly process and material enhancements for flip chip packaging of low-k devices. Underfill choice is the single most important choice in flip chip packaging of low-k devices. A high modulus underfill must be avoided to keep from transferring too much of the stress induced by substrate to die expansion coefficient mismatch to the low-k. A high modulus underfill results in low-k delamination in temperature cycle.

However, very low modulus underfills must also be avoided because low modulus underfills transfer too much stress to the flip chip bump which results in bump cracking in temperature cycle.

Amkor has qualified one primary underfill for low-k. The basic parameters of this underfill are:

- Low Alpha 1
- Low Tg
- Moderate Modulus

This approach is accepted in the industry and has the largest first level (flip chip bump interconnect) reliability data base.

Initially, most data gathered by the industry on low-k flip chip utilized eutectic bumps. This is because eutectic bump is the most common bump for organic substrates. High Pb bumps have higher resistance to electromigration. Electromigration is only an issue for high current density applications. The lower modulus, lower Tg underfills that are used for low-k die exert less stress on the die surface but this stress is transferred to the bumps. Eutectic bumps are strong enough that no decrease in temperature cycle life has been able to be measured. However, high Pb bumps can crack more easily if the solder mask opening on the substrate is narrow and creates 'necking' in the bump. Therefore, Amkor increases the solder mask opening for high Pb bumps on organic substrates with low-k, compensating for the low-k underfill.

With successful qualification and production of eutectic and high Pb bump on low-k, focus migrated to lead-free bump on low-k. Full lead-free low-k is now qualified using Amkor (UST) Sn2.3Ag bump up to 15mm die size.

The European Directive for Restriction of Hazardous Substances (RoHS) in Europe currently allows the use of high Pb bump until 2010. Use of eutectic bump is expected to be exempted in early 2006.

Amkor has an extensive reliability data set on low-k devices packaged in *Super*FC® construction. This data can be found in the low-k Flip Chip presentation. For a copy, please contact your Account Manager.

Amkor does not recommend backgrind (wafer thinning) of large low-k die. Initial data supports better reliability with thicker wafers.

Important assembly process modifications have been made for low-k. Most 0.13um and 90nm low-k wafers have 80um wide streets. The seal ring peripheral structure on the die protects the die in most cases from saw induced damage, stopping passivation peeling and chipouts from entering the active die area.

However, Amkor recommends that customers also implement a "keep-out" area where no metal is allowed in the saw street within 0.5mm of the die corner and increase saw street width when possible. Narrower saw blades are used on low-k devices to minimize the risk of chip-outs into or past the seal ring. Saw feed rate is also slowed to minimize clogging of the saw blade 'teeth' with sawn detritus from the saw street. This is particularly important with saw streets with heavy metal loading.

Thus, when a customer requests a low-k build, it is very important to inform the factory that the wafer is a low-k wafer by specifying the dielectric type on the pull down menu on the Customer Build Request Sheet.

The optimum saw street configuration is to increase the saw street to 160um and move all street metal to one side of the street, enabling a metal free saw path on one side of the street.

Amkor is in production on low-k flip chip. low-k volumes have ramped significantly during 2005 and 2006. For further information, contact your flip chip customer Account Manager or David McCann. David can be reached at 480-821-5000 x5029 or dmcca@amkor.com