Achieving the 3rd Generation From 3D Packaging to 3D IC Architectures

Lee Smith
Amkor Technology Inc.

Abstract

3D packaging is entering the third generation of technology architecture as full 3D IC stacks with through silicon via (TSV) and flip chip micro-bump interconnects. This article will summarize the role industry collaboration played in enabling the first two generations of 3D packaging architectures – stacked die and stacked packages – specifically noting where collaboration was key to resolving the business and logistic challenges that impact design, integration, interconnect or infrastructure development for mass production. Emerging 3D IC architectures and supply chains face greater technical and business model challenges. Understanding the lessons learned in past 3D architectures may enable new approaches to effective collaboration.

3D Packaging Market Summary

In 2009, industry analysts estimated nearly 5 billion 3D packages were integrated into electronic systems. This represents over 3 percent of the total IC package units and 11 percent of the chip-scale packages produced last year. 3D package architectures, including stacked die and stacked PoP, were prevalent on all analysts' lists of the fastest-growing package technologies from both historical and forecast perspectives. Die stacking has achieved critical scale on lead frame and organic laminate substrates using both multi-tier wirebond and flip chip + wirebond interconnects. The stacking of TSOP packages has seen renewed demand for higher NAND density in applications including solid state drives. Strong demand in smartphones for logic + memory 3D integration has driven wide adoption of laminate-based PoP stacks with both wirebond and FC interconnects used for the bottom logic device, and wirebond stacked die for the top memory package.

Increased memory density, RAM + non-volatile memory combinations, mixed signal, logic + memory and ASIC + MEMS sensor stacks represent the majority of devices integrated in 3D packages. Mobile phones, handheld multimedia systems and

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solid state storage devices utilize 3D packaging technologies to integrate more of these devices in the smallest form factor. Systems designers use metrics such as the number of MIPS or megabytes per cubic millimeter to evaluate 3D package architectures.

First-Generation 3D: Stacked Die Packaging

Stacked die combination memory packages evolved in the late '90s driven by mobile phone requirements for 3D integration of NOR flash and SRAM devices in a stacked chip-scale package. Figure 1 (from the presentation of an Amkor and Sharp joint Pan Pacific 2000 paper[1] illustrates the Stacked CSP (S-CSP) architecture.

The foundation for high-growth standard S-CSP components was laid through collaboration between NOR flash and SRAM device suppliers formalized in 1998. Collaboration included business agreements for wafer supply of known good tested devices and development of industry standards for the mechanical outlines and memory pinouts for S-CSP combo memory components.

S-CSP requirements drove collaboration with equipment, substrate and material suppliers to development process innovations in thin core 2 layer substrates, wafer thinning/handling, die attach, thin die stacking, low loop wire bonding and low-profile molding technologies. Business agreements ensured significant investments for scale-up of IC suppliers' internal and outsourced package assembly and test lines for S-CSP. Strong collaboration has continued over the past decade to address low-power DRAM, NAND and logic stacked die integration requirements. Flip chip attach has been integrated in stacked die assembly lines for form factor and electrical performance requirements driven by the integration of advanced logic,

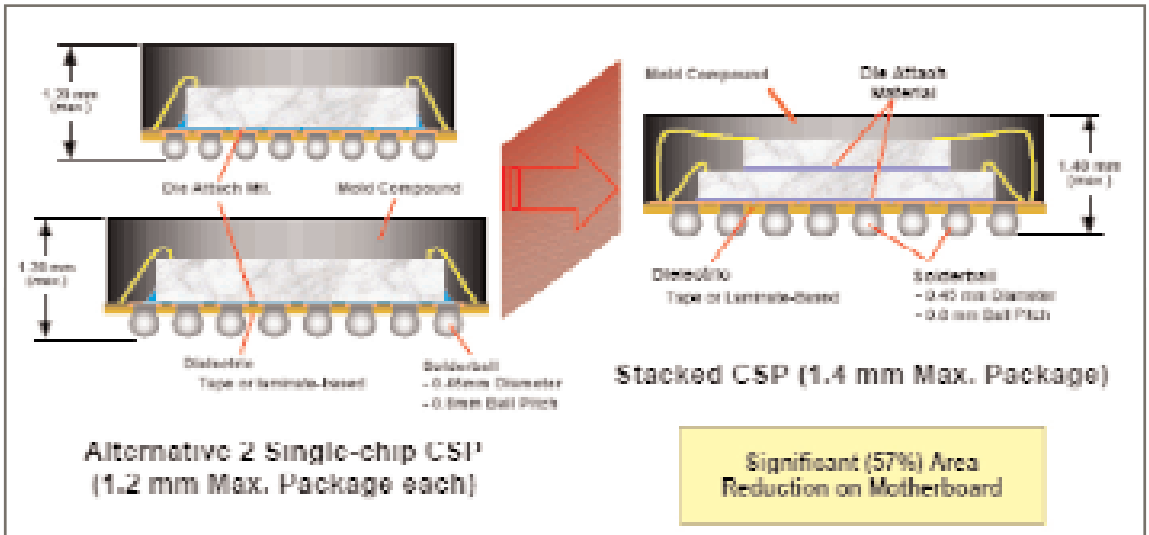

Figure 1. Flash + SRAM Integrated Into S-CSP

mixed signal and RF devices in the stack. From this joint work, the industry delivered over 3 billion stacked die package units last year, with approximately 8 billion devices integrated. FC + wirebond die stacks have reached critical mass. Densities up to nine die stacks are shipping in high volume and suppliers have demonstrated 18 to 24 die stack capabilities with die thicknesses below 25 micrometers using thin die attach films, low loop wire bonding and advanced molding technologies.

Second-Generation 3D: Stacked Package-on-Package (PoP)

The business and logistics challenges associated with the scalability of stacking leading-edge logic and combo memory die within one package led to collaboration projects between Nokia and Amkor to develop a stacked package platform solution. As a result, the scope of collaboration expanded significantly for the PoP architecture, as system designers and SMT process engineers were key participants in the development of PoP. Following the initial technology platform work, reported in 2002[2] and 2003,[3] a new development project was initiated with an expanded collaboration team that include key logic and memory device suppliers. This team was challenged by the mandate to develop and deploy a package stack architecture for a new phone launch, against a fixed schedule. In addition, the package stack solution had to meet technology platform requirements so that it could be applied to a wide range of emerging logic + combo memory stacking requirements. I was honored to lead this team that was able to deploy PoP into production just 15 months from agreement on the package stack platform architecture and memory interface, meeting or exceeding all of the project milestones. PoP co-development demonstrated the huge benefits possible through strong collaboration and that clear project requirements can overcome cultural and communication challenges across four companies on three continents spanning the full supply chain. Each company was able to enjoy market leadership in PoP technology to address the explosive adoption in mobile multimedia applications, which I summarized in a previous industry article.[4]

As described for stacked die, the PoP architecture is evolving rapidly to address higher interconnect densities in thinner, flatter PoP stacks. Figure 2 shows the PoP stacked structures that have been prevalent in handsets over the last five years, where the top package solder balls provided SMT stacking clearance over the bottom wire bonded or FC logic die.

Strong industry collaboration was critical in expanding the infrastructure, including JEDEC standards for PoP that enabled

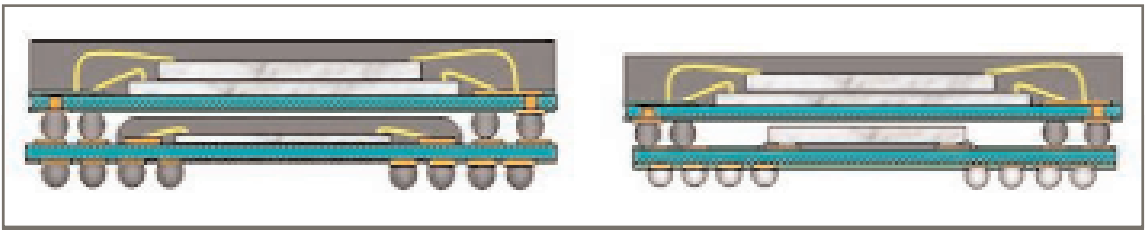

Figure 2. First Generation of PoP Stacked Structures

over 200 million PoP stacks to be integrated within handsets last year achieving adoption by every smartphone maker in the world.

However, now the requirements for logic and memory device technologies are transitioning to higher data rates and wider bandwidths, thereby driving an increase in pin counts, interconnect densities and electrical performance requirements. This is driving a strong transition to mobile processor devices fabricated on advanced 45-28nm CMOS wafers with low-k dielectric layers and flip chip interconnects. Designers require a bottom package technology that can support integration of flip chip, stacked die, decoupling capacitors and new fine-pitch, high-density memory interfaces. This first generation of PoP structures is not able to meet these new performance requirements, so a new PoP architecture is required that can scale with the evolving bottom package integration and density requirements. I summarized these requirements, and an emerging high-density PoP solution was summarized in an article two years ago.[5] What has not been reported yet is the strong collaboration involved in the development, certification and deployment of a new high-density PoP platform for the next-generation requirements.

Collaboration for Through Mold Via (TMV) PoP for Next-Generation High-Density Applications

The application of solderable package stacking vias through the bottom package mold cap was first reported at the 2008 Electronic Components and Technology Conference by Kim et al.[6] as a new

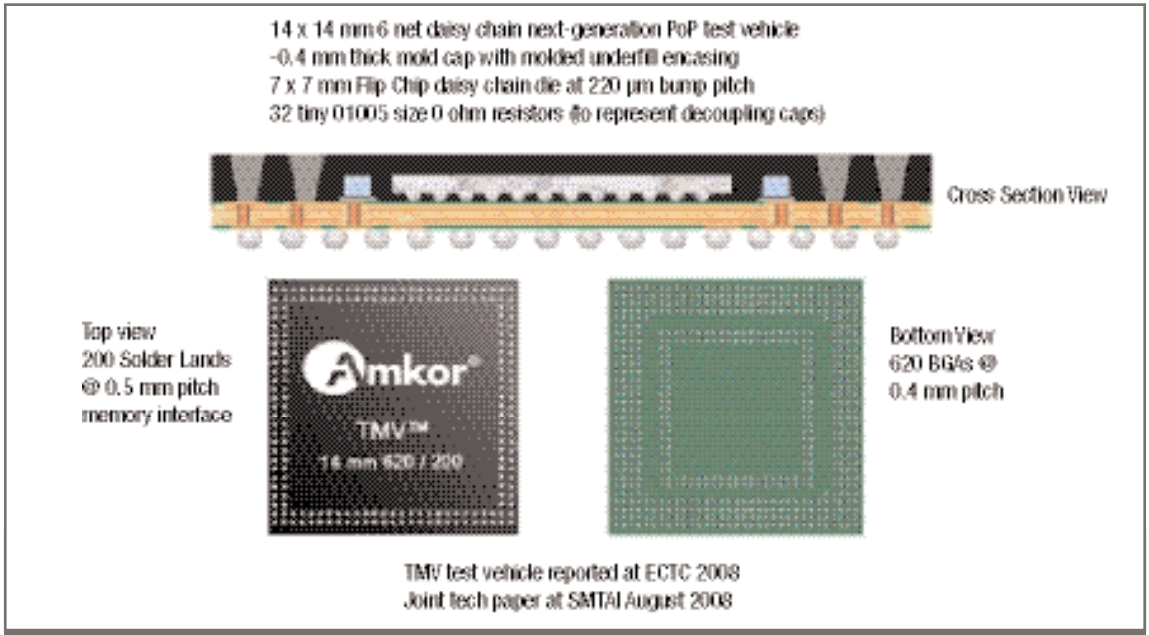

Figure 3. Bottom TMV PoP test vehicle as reported at ECTC and SMTAI in 2008.
(Top memory package would be surface mounted in applications, but not shown in this figure).

bottom package structure and assembly method for fine-pitch PoP requirements with improved warpage control. Following this paper, a series of joint papers were reported to characterize surface-mount stacking of this new PoP platform and qualify the board-level solder joint reliability. For internal qualification and industry collaboration projects, a high-density 14 x 14 mm multi-net daisy chain test vehicle was developed with 620 bottom BGAs at 0.4 mm pitch and 200 stacked TMV solder joints at 0.5 mm pitch. Figure 3 shows the cross section, top (TMV) and bottom (BGA) patterns of this daisy chain test vehicle. The first collaboration project where industry publication was approved was joint work with Sony Ericsson Mobile Communications at the SMTA International conference in August 2008.[7]

The following year, two additional joint projects were published to characterize smaller and thinner TMV PoP structures. The first joint project for a 12 x 12 mm TMV PoP structure was one with ST Microelectronics and Nokia, reported at the European Microelectronics and Packaging Conference (EMPC).[8] The second joint project where industry publication was approved was a follow-on to the 14 mm 620/200 test vehicle shown in Figure 3, which did not require the integrated passive devices, so was able to support a thinner 0.25 mm mold cap necessary to meet thin PoP stack up requirements. The scope of this project included SMT yield characterization of both flux and paste dip stacking processes. This was a joint project between Amkor and Celestica reported at SMTA International October of 2009.[9]

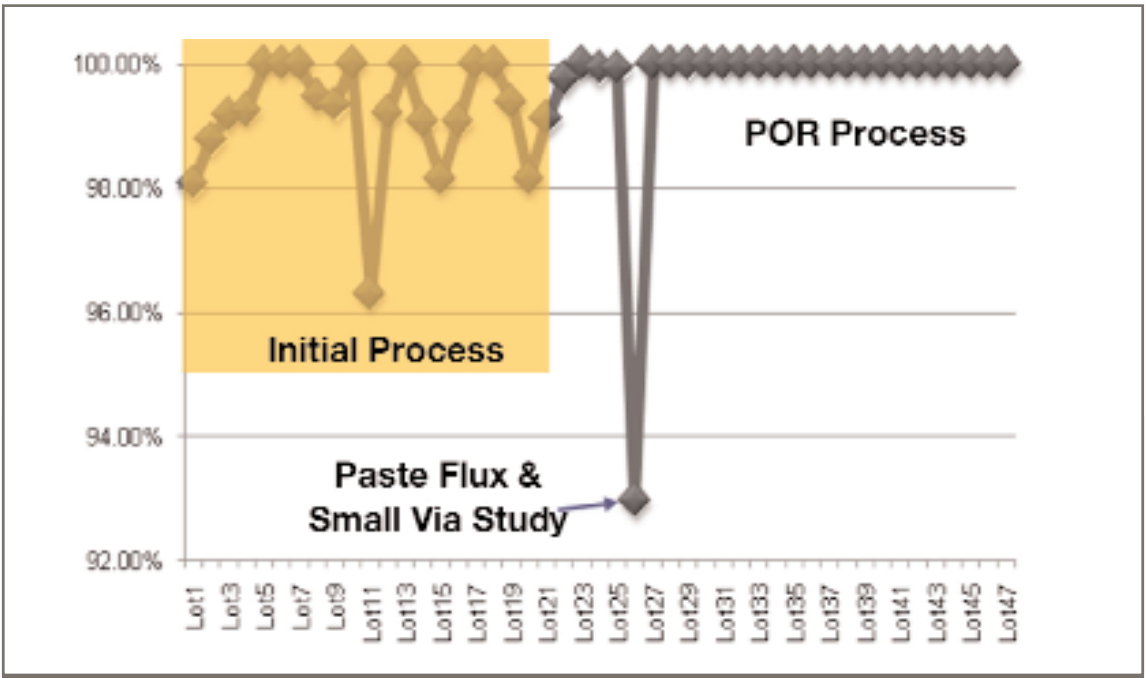

Figure 4. SMT Yield Plot of TMV PoP Stacking Studies

In addition to this joint work approved for publication, Amkor supported a range of proprietary or alpha customer development and qualification joint projects for TMV PoP applications. The alpha customer project included work to demonstrate stable 100 percent SMT stacking yields based on continuity testing. Figure 4 illustrates the inconsistent SMT yield associated with the initial TMV and SMT processes versus the stable 100 percent stacking yields achieved on lots 27 through 47 following optimization of the TMV fabrication and SMT stacking processes. The lot sizes varied based on the scope of the study. In total we stacked over 50,000 units in this work, and customers have been satisfied the plan of record (POR) process offers stability for high-volume manufacturing SMT requirements. This work and data was reviewed with the alpha customer during the scope of the study, and then a summary was presented at the IMAPS Device Packaging Conference in March 2010.[10]

Third-Generation: 3D IC Considerations

Collaborate, collaborate, collaborate!

A majority of the 8-9 billion ICs integrated in 3D packages last year were not designed for stacking and are typically offered as single-chip as well as 3D-packaged components. When performance or integration raise significant challenges or the 3D architecture becomes the dominant application, then we see new chips floor plans designed for the 3D package requirements. This approach is not an option for 3D IC architectures where the TSV interconnection structure is a key element of IC design and heterogeneous device integration. So for 3D IC development, the industry has formed a number of groups to collaborate on technical challenges from design through process and materials development. The first area for strong collaboration is in the design phase, which includes the following activities:

- The Global Semiconductor Alliance (GSA) has formed an EDA Interest Group to work on 3D/TSV design tools and solutions. They will be presenting their work at DAC 2010.
- JEDEC has technical groups working or forming to develop mechanical and electrical standards for TSV technology in memory (JC-42) and multi-chip applications (JC-63).

Design rules can have significant impact on 3D IC structural integrity, creating process and material interactions between the thin chips, micro-bump FC stacks and package interfaces, which can impact quality and reliability. As a result, strong worldwide collaboration efforts have been under way for a couple of years in the TSV process, materials and technology areas, including the following few examples:

- EMC-3D consortium created in October 2006 to "address the technical and cost issues of creating 3D interconnects using TSV technology for chip stacking and MEMS/sensors packaging." The consortium includes equipment, materials and technology members. For more information, see www.emc3d.org.
- Korea Advanced Institute of Science and Technology (KAIST) is an EMC-3D member and has a 3D IC/TSV consortium within Korea, of which Amkor Technology is a member.
- Imec (Interuniversity MicroElectronics Center) has development collaboration projects over various aspects of 3D integration technologies with TSV

interconnects. For more information, see www2.imec.be.

- ASET (Association of Super-Advanced Electronics Technologies) is specific to Japanese companies but has broad participation across the 3D supply chain from systems to materials. For more information, see www.aset.or.jp.

Conclusion

Industry collaboration has been critical in 3D packaging architectures to address the technical, business and logistics requirements for integration of multiple devices. Strong collaboration is more critical to achieve the challenging cost, performance and reliability requirements with 3D IC architectures using TSV interconnects. The collaboration efforts over the past three to four years are bearing fruit, and commercialization of 3D IC components are emerging in stacked DDR and other high-performance applications.

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About the Author

Lee Smith

Lee Smith is an industry expert in 3D packaging, with 30 years of diverse technology and market development experience in folded flex, stacked die and stacked packages. Over the past 13 years, he has held 3D packaging technology and business development responsibilities at Amkor, Texas Instruments and Tessera, with market emphasis in mobile handsets. Lee is recognized for leading the technology and infrastructure development of the widely adopted package-on-package (PoP) architecture. ■

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