

# Packaging a 40-Gbps Serial Link Using a Wire-Bonded Plastic Ball Grid Array

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*Editor's note:*

System in package provides highly integrated packaging with high-speed performance. Many SiP packages contain low-cost 3D stacked chips interconnected by fine wire bonds. In a high-frequency spectrum, these wire bonds can cause discontinuities causing signal degradation. This article addresses problems with wire bonding in high-frequency SiP packages and proposes design methodologies to reduce these discontinuities.

—Bruce C. Kim, University of Alabama

Previous work has studied the use of WB-PBGA packages for up to 10-Gbps data rates.<sup>5,6</sup> Despite the concerns of high-frequency loss in a WB-PBGA package, we believe it's possible to design a 40-Gbps package with that technology. Because such a high speed is beyond the reach of conventional design, we propose new design methodologies.

■ **ADVANCES IN CMOS TECHNOLOGIES** let the number of transistors grow much more rapidly than the number of I/Os.<sup>1</sup> This huge discrepancy in growth rates means that the bandwidth of each I/O pin becomes more critical as technology scales down.<sup>2</sup> Processors' increasing computational capability is driving a need for high-speed links to communicate the processed information.

For the past 10 years, research on these links has focused on improving transceiver circuits to sustain desired data rates.<sup>3,4</sup> Although this has led to expectations of continued data rate advancements, the nature of link design is changing. Today's internal circuits can run at tens of gigabits per second (Gbps), but the bandwidth of the channel—the physical medium through which the signal propagates from transmitter output to receiver input—limits link performance.

Among channel components, the package is becoming a major bandwidth constraint.<sup>5,7</sup> As data rates continue to increase, transitioning to flip-chip interconnects or low-loss substrate materials results in excessive cost.<sup>7</sup> It is therefore increasingly important to provide a high-performance and low-cost packaging solution.

Wire-bonded plastic ball grid array is the most popular package for cost-effective conventional midspeed appli-

## Discontinuity cancellation

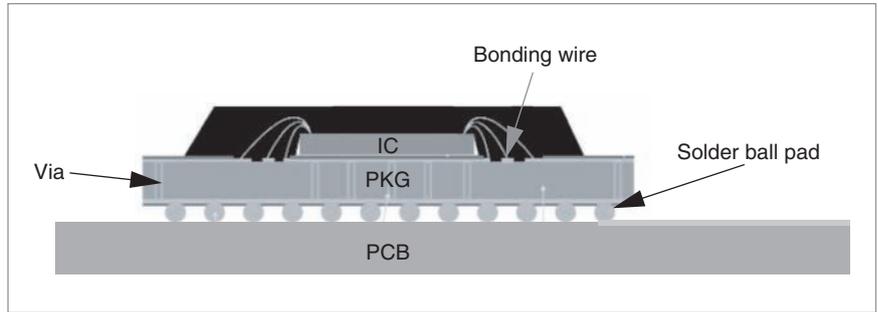
Figure 1 shows a channel in a WB-PBGA package, consisting of bonding wires, package traces, vias, and balls. The package traces form uniform transmission lines whose bandwidth depends only on the substrate material's property. Thus, a straightforward solution to extending the bandwidth further is to invest in low-loss materials. However, the other components' bandwidths depend on the 3D structure's design, giving designers room to display their creativity.

A capacitance or inductance produces reflection when it impairs a transmission line. The combined reflection of both effects is less than the sum of the amplitudes of the individual effects because they have opposite polarities. A first-order model handles this partial cancellation by reducing the original configuration to a single value of either excess capacitance or excess inductance, according to which effect creates greater reflection.<sup>8</sup>

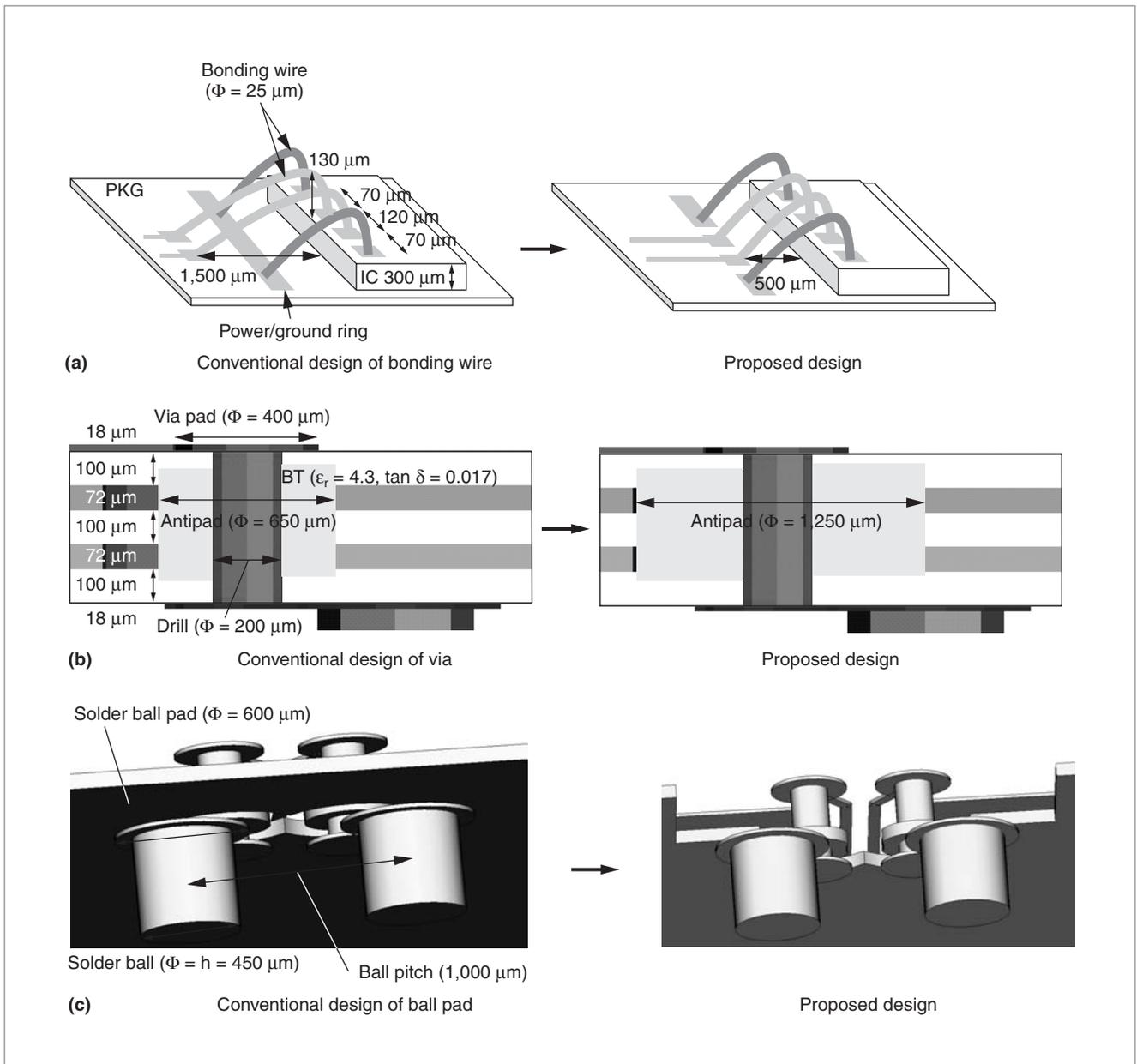
Reflections occurring in the channel degrade the bandwidth. To avoid reflection, a straightforward solution is to shrink the discontinuity's physical dimension, thereby decreasing its inductance and capacitance simultaneously. However, the feasibility and reliability of packaging technologies prevent designers from mak-

ing the dimension sufficiently small.

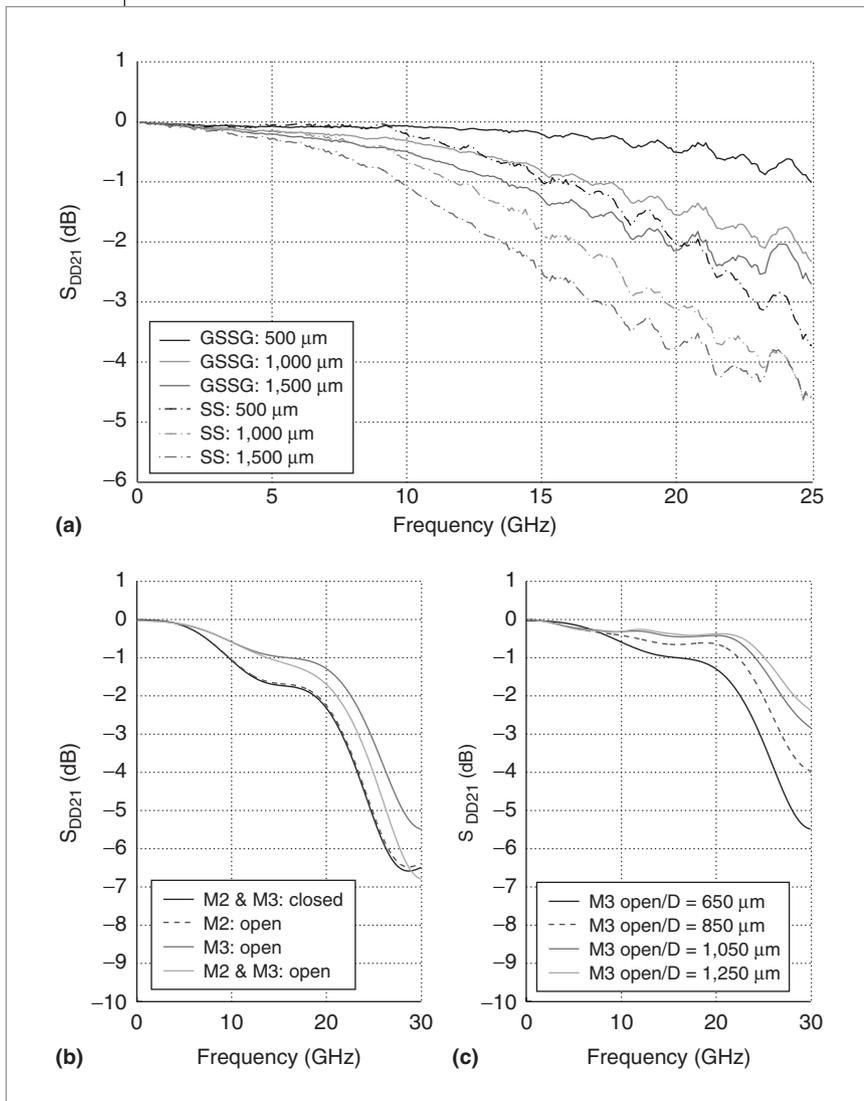
A more feasible solution is to balance the capacitance with the inductance, thereby canceling any excess reactance. We can accomplish this discontinuity cancellation by controlling the distance between the discontinuity and the neighboring reference plane. For example, if we decrease the distance, the capacitance increases while the inductance decreases.



**Figure 1. Three discontinuity regions in a wire-bonded plastic ball grid array package.**



**Figure 2. Proposed design methods using bonding wire (a), via (b), and ball pads (c) for discontinuity cancellation.**



**Figure 3. Effect of bonding wire length and configuration on channel bandwidth, where GSSG is a ground-signal-signal-ground configuration, and SS is a signal-signal configuration (a); the removal of the metal pieces of inner planes above the ball pads (b); and an increase in the antipad diameter on the channel bandwidth (c). M2 and M3 are the second and third metal layers, respectively.**

#### Package design methodology

Figure 2 shows the three discontinuity regions that we investigated in a WB-PBGA package using full wave simulation with a typical dimension. We extracted equivalent circuit models from the simulation results.<sup>9</sup> We categorized each region based on the model parameters, and we proposed corresponding design methods for the discontinuity cancellation.

Figure 2a shows the bonding wire, which we categorized as the inductive region. Because the bonding

wire's differential impedance is larger than 100 ohms even with the minimum pitch between the ground and the signal wire, discontinuity cancellation isn't possible. Instead, we minimize the length to mitigate excess inductance. Conventional designs have used power and ground rings on which power and ground wires land. Signal wires are considerably longer because they jump over the rings. Thus, we can place bonding pads as close as possible to the die edge by cutting those rings around critical signals.

A via is a transition from a top layer to a bottom layer; it features a via pad at the top and bottom of a cylinder (drill) that passes through openings (antipads) in inner planes. We categorize a via as a capacitive region because of the capacitance between the drill and the inner planes. To adopt the discontinuity cancellation here, we increase the antipad's diameter, as Figure 2b shows.

Short, wide traces of a teardrop shape connect vias to ball pads. This section tends to be capacitive because of the large capacitance caused by an upper plane. We can apply the discontinuity cancellation to this section by removing the metal piece of inner planes above the ball pads, as Figure 2c shows.

#### Effect on channel bandwidth

We analyze each proposed design method's effect on channel bandwidth. Figure 2 shows the bonding wire, via, and ball pad dimensions of the package we studied. The channel starts where the bonding wires connect to die pads, and terminates at the junction between the ball pads and the underlying PCB, including the 5-mm package trace on the top layer.

To investigate the bonding wire length's effect, we measured a test vehicle with bonding wires of various lengths using a four-port network analyzer and microprobes. As Figure 3a shows, a shorter wire experiences less insertion loss. Adding a ground wire on each side of the signal wires is essential for reducing excess inductance. Assuming a fixed total length, package traces become longer as bonding wires become shorter.

Because the package traces form uniform transmission lines, if properly designed, they are far less damaging than the bonding wires. Therefore, the bonding wire length should be minimized, and our proposed design method of cutting power and ground rings achieves this.

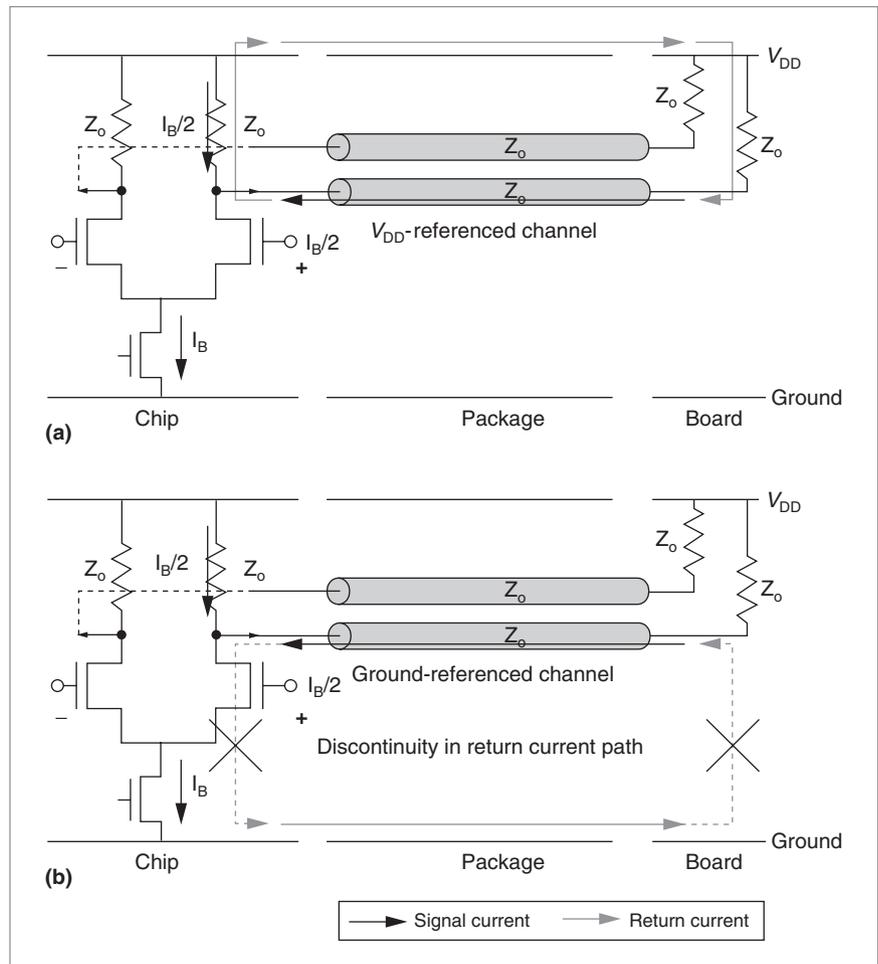
We next analyzed the ball pad. Figure 3b shows the results of our first modification of a conventional design (M2 and M3: closed), which was to remove the metal piece of the third layer closest to the ball pads (M3: open). As the graph shows, digging out the metal piece improves the channel bandwidth. Further removal of metal pieces from both inner planes (M2 and M3: open) degrades the channel bandwidth because of excess inductance, resulting from an overly reduced capacitance. On the other hand, the “M2: open” case shows no difference from the conventional design because the third layer screens the second layer.

Figure 3c shows the effect of increasing the antipad diameter for the “M3: open” case. The combined effect of the two discontinuity cancellation techniques appears considerable. This is a remarkable achievement because they add no cost, and are thereby free from the cost-performance trade-off. To achieve an excess capacitance of 0 for each discontinuity, we uniquely determine the area of the metal piece to be removed and the antipad diameter.

## Return-current-path design

For every signal current, there is an equal and opposite return current. The concept of return current is a 1D circuitual interpretation of 3D field-propagation phenomena that are more complex to visualize. Return current is as important as signal current for signal integrity. However, a common mistake is to focus on providing a clean and controlled signal trace, with no thought as to how the current will return.<sup>10</sup>

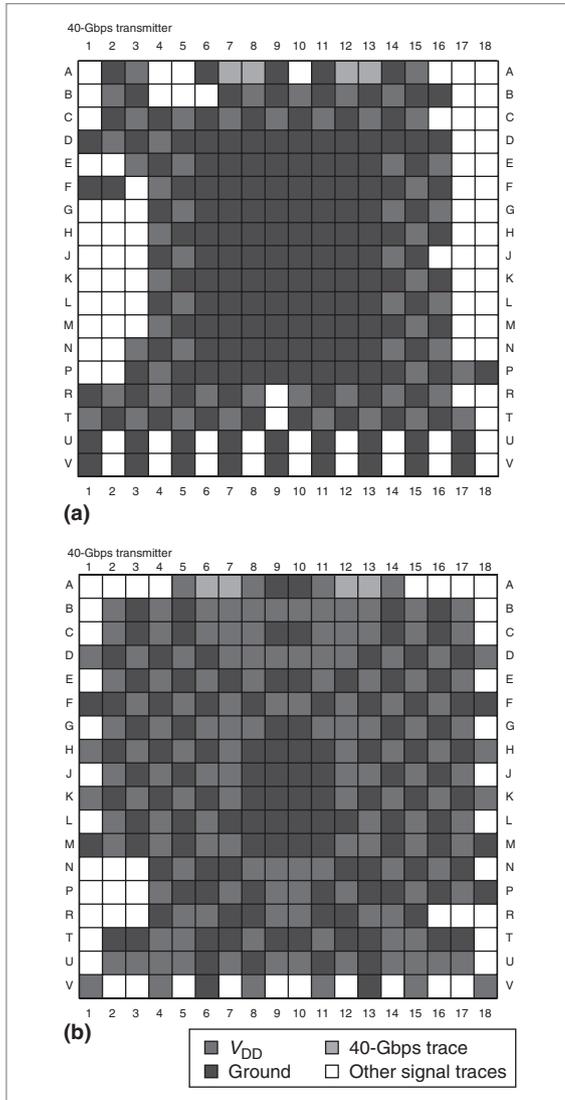
Any current injected into a system must return to a source, thereby completing a loop. In a simple output buffer of inverter type driving a ground-referenced line, instantaneous currents occur when the driver switches from low to high. As the signal current propagates down



**Figure 4. Return-current path of current mode logic buffer driving a  $V_{DD}$ -referenced channel (a) and a ground-referenced channel (b).**

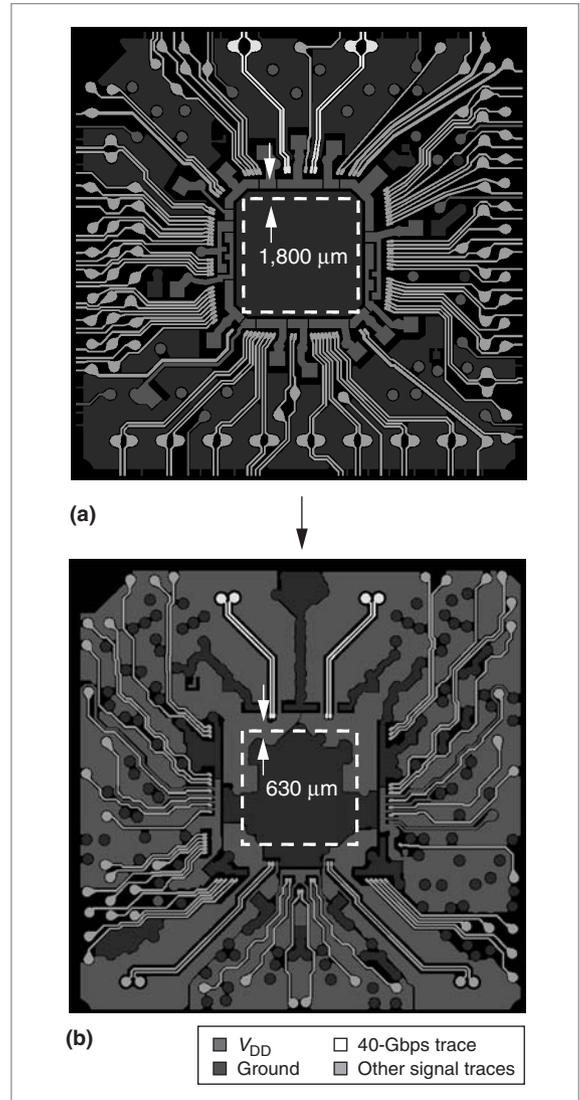
the line until it is charged up to  $V_{DD}$ , the return current is induced on the ground rail, which flows in the opposite direction. At both ends of the line, the current must find the path of least impedance to complete a loop, which can be a system voltage regulator module at low frequency, or decoupling capacitors on a board and a package at mid frequency, or on-chip decoupling circuitry at high frequency. Therefore, designing a return-current path is in the long run equivalent to designing a power distribution network (PDN). Furthermore, designers should consider the entire hierarchy of chip-package-board concurrently to capture the return current's behavior correctly.

The return-current path also depends on the I/O schematics. Current mode logic (CML) drivers have recently become popular for high-speed serial links.<sup>4</sup> Figure 4a illustrates the return-current path of the CML buffer driving a  $V_{DD}$ -referenced channel. The sig-



**Figure 5. Ball map design: previous design, where ground is the second layer and composes the inner ring, and where the  $V_{DD}$ :ground ratio is 63:174 (a); and our proposed design, where we assign the second layer and inner ring to  $V_{DD}$ , with a  $V_{DD}$ :ground ratio of 146:127 (b).**

nal current (black line) and the return current (gray line) form a loop through the termination resistors. Figure 4b shows the return-current path of the same buffer driving a ground-referenced channel. Return-current path discontinuities exist at both ends. In a real PDN, decoupling capacitors bypass the return current, but that path is also considerably inductive. Therefore, in our use of the CML buffer, we route a channel with reference to  $V_{DD}$  by choosing the stack-up appropriately.

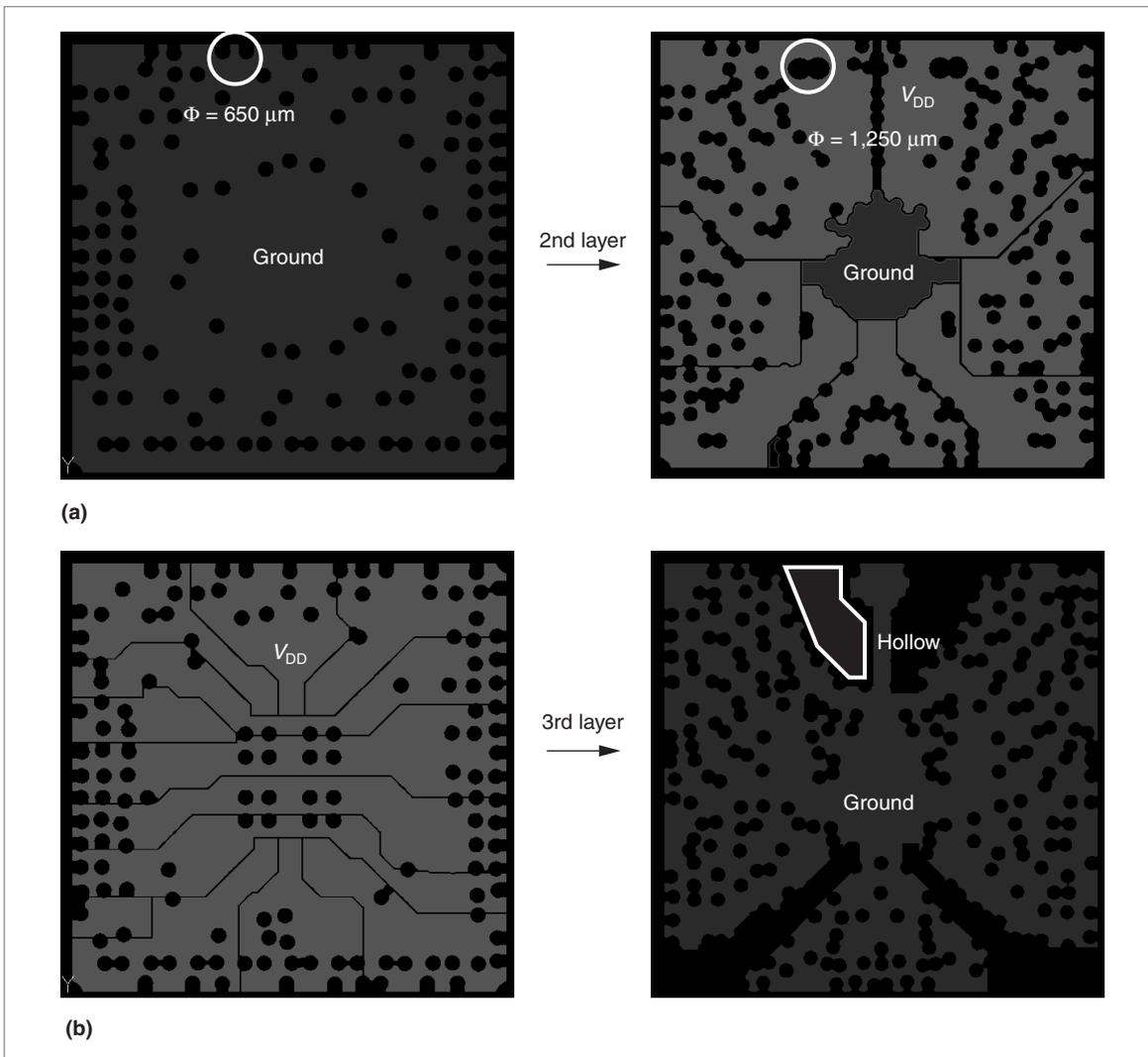


**Figure 6. Bonding wire design: previous design (a); proposed design (b).**

### Application to a 40-Gbps package design

We designed two versions of four-layer WB-PBGA packages, one according to the proposed methodologies, and the other conventionally. Both versions have the same body size (19 mm  $\times$  19 mm), the same ball count (18  $\times$  18 full array), and the same material (bismaleimide triazine). The only difference is the electrical design.

As we demonstrated earlier, a channel for a high-speed serial link using a CML buffer should reference a  $V_{DD}$  plane. Because most of the return current flows along the  $V_{DD}$  plane, we reduce the inductance of the path on that plane by allotting more pins. Figure 5 compares ball map designs. In the proposed design, we



**Figure 7. Via and ball pad design. For the proposed design, we increased the antipad diameter (a), and removed the metal plane above the ball pad (b).**

assign the second layer to  $V_{DD}$ . Furthermore, the number of  $V_{DD}$  balls is greater than the number of ground balls. Finally, we also assign an inner ring to  $V_{DD}$ .

We cut the ground ring around the 40-Gbps pins and placed the bonding pads as close as possible to the die edge (white dotted line), as Figure 6 shows. Furthermore, the 40-Gbps traces are wholly guided by the  $V_{DD}$  plane, whereas in the previous design the 40-Gbps traces suffer from reference plane change.

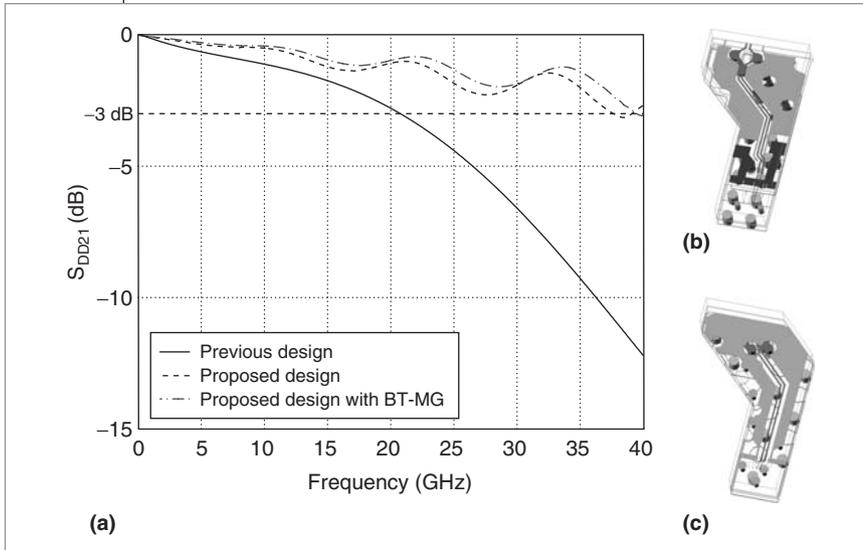
For the 40-Gbps pins, we increased the antipad diameter from 650 microns to 1,250 microns, as Figure 7a shows, and removed the metal piece of the third layer above the ball pads (Figure 7b).

Figure 8 shows the post-layout simulation results for the two designs. We increased the channel bandwidth

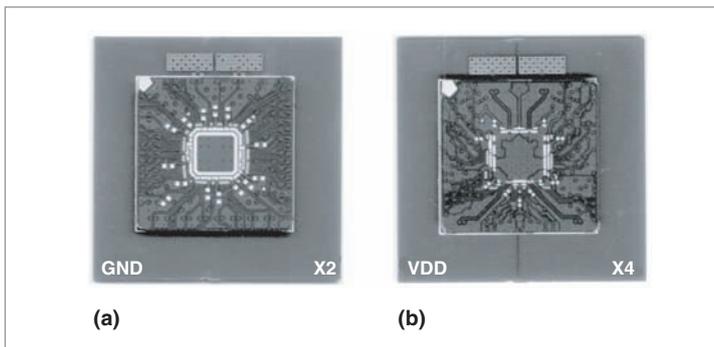
by a factor of 2, simply by modifying the electrical design according to the proposed methodologies, with no increase in cost. Further improvement using low-loss material should be relatively insignificant. This means that there is much room to further optimize the WB-PBGA package's electrical design before transitioning to ceramic packages or other advanced packaging technologies.

We manufactured and assembled the two package designs with a dummy silicon and a board, as Figure 9 shows. The die has pads only for wire bonding and probing. The board has a BGA footprint, short traces, and pads for probing. We implemented both on an FR4 substrate using PCB technology.

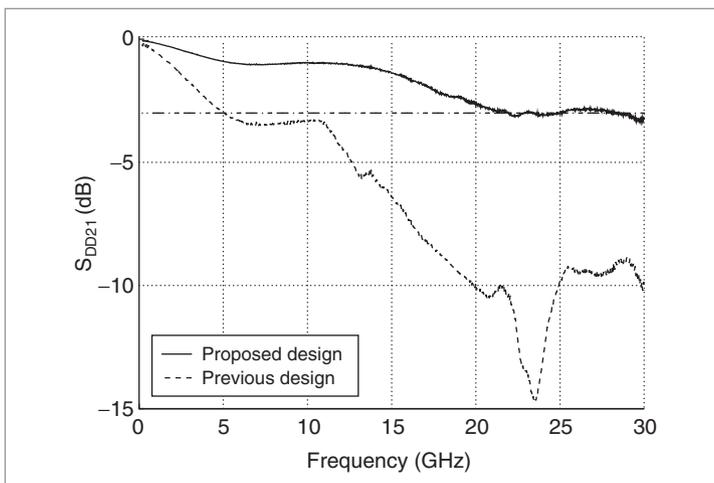
We measured the entire channel performance,



**Figure 8. Post-layout simulation results (a) for previous (b) and proposed (c) designs.**



**Figure 9. Photographs of assembled package and board (die is not shown): previous design (a), and proposed design (b).**



**Figure 10. Comparison of measured results for overall channel performance.**

including the bonding-wires effect, using a four-port network analyzer and micro-probes. As Figure 10 shows, we measured the previous design's insertion loss above 10 dB at 30 GHz. A resonance occurs even at around 23 GHz, where the insertion loss increases up to 15 dB. However, the proposed design's insertion loss is below 3.5 dB at up to 30 GHz, and the 3-dB frequency is higher than 20 GHz. Furthermore, there is no resonance, meaning the signal does not feel any severe discontinuity when passing through the package. The proposed design shows remarkably enhanced performance over the previous design.

**BY AVOIDING** the use of low-loss dielectric material or advanced packaging technology, our WB-PBGA package can provide a low-cost packaging solution for future high-speed serial links. Although our consideration in this article is limited to WB-PBGA packages, we could readily apply the proposed design methodologies to advanced packaging technologies, further improving channel bandwidth. ■

## References

1. W. Dally and J. Poulton, *Digital Systems Engineering*, Cambridge Univ. Press, 1998.
2. H. Hofstee, "Future Microprocessors and Off-Chip SOP Interconnect," *IEEE Trans. Advanced Packaging*, vol. 27, no. 2, 2004, pp. 301-303.
3. C. Yang and M. Horowitz, "A 0.8- $\mu\text{m}$  CMOS 2.5-Gbps Oversampling Receiver and Transmitter for Serial Links," *IEEE J. Solid-State Circuits*, vol. 31, no. 12, 1996, pp. 2015-2023.
4. J. Kim et al., "Circuit Techniques for a 40-Gbps Transmitter in 0.13- $\mu\text{m}$  CMOS," *Proc. IEEE Int'l Solid-State Circuits Conf. (ISSCC 05)*, 2005, pp. 150-151.
5. X. Zhou and N. Fang, "Performance of Low-Cost PBGA Package for 10-Gbps Applications," *Proc. IEEE Topical Meeting on Electrical Performance of Electronic Packaging (EPEP 02)*, IEEE Press, 2002, pp. 71-74.
6. R. Emigh, "Electrical Design for High Data Rate Signals in Conventional, BT-Based PBGA Substrates Using Wire Bonded Interconnection," *Proc. IEEE Electronics Packaging Technology Conf. (EPTC 03)*, IEEE Press, 2003, pp. 517-522.
7. L. Shan et al., "Simulation and Design Methodology for a

50-Gbps Multiplexer/Demultiplexer Package," *IEEE Trans. Advanced Packaging*, vol. 25, no. 2, 2002, pp. 248-254.

8. H. Johnson and M. Graham, *High-Speed Signal Propagation—Advanced Black Magic*, Prentice Hall PTR, 2003.
9. D. Kam et al., "Twisted Differential Line Structure on High-Speed Printed Circuit Boards to Reduce Crosstalk and Radiated Emission," *IEEE Trans. Advanced Packaging*, vol. 27, no. 4, 2004, pp. 590-596.
10. S. Hall et al., *High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices*, John Wiley & Sons, 2000.



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