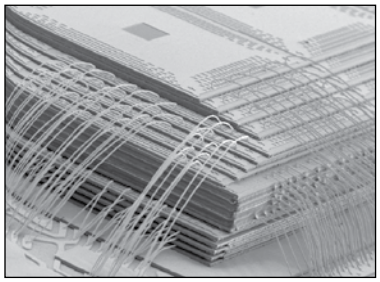
Technology Solutions

3D & Stacked Die Packaging



3-dimensional (3D) packaging technologies exploit the third or Z-height dimension to provide a volumetric packaging solution for higher integration and performance. 3D packaging has become critical to integrating the multi-media features consumers demand in smaller, lighter products. This increasing functionality requires higher memory capacity in more complex and efficient memory architectures.

New product designs (cell phones, digital cameras, PDAs, audio players and mobile gaming) demand that these features be delivered in innovative form factors and styling. 3D packaging is experiencing high growth and new applications by delivering the highest level of silicon integration and area efficiency at the lowest cost.

3D Packaging Innovation

Since 1998, Amkor Technology has been a pioneer in developing and providing high volume, low cost 3D packaging technologies. Amkor understood the benefits that 3D packaging provided which would address a wide range of device combinations and end product applications.

A platform technology development through deployment approach was created to transcend the range of applications and packaging platforms requiring 3D technology. Customers continue to benefit from this approach as new 3D packaging solutions are more effectively qualified and ramped to high volume, at low cost and across multiple factories.

The critical 3D platform technologies include:

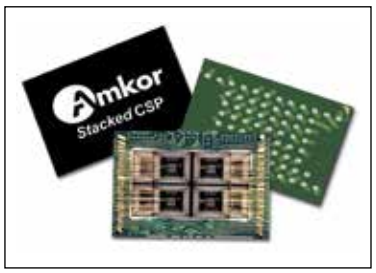
- Design rules and infrastructure for thinner, high density substrate technologies
- Advanced wafer thinning and handling systems
- Thinner die attach and die stacking processes
- High density and low loop wire bonding
- Pb-free and environmentally conscious "Green" material sets
- Flip chip plus wire bond mixed technology stacking
- Turnkey die and package stacking assembly and test flows

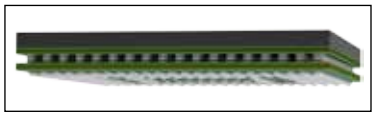
Benefits of Three Dimensional Packages

The high growth and development of multiple 3D packaging technologies are due to the system level benefits provided, including:

- Size and weight reduction through more semiconductor functions per cm^2 of PWB space and cm^3 of application space
- Enables more design freedom to create innovative new form factors and styling through volumetric packaging approach
- Enables higher electrical performance through shorter interconnect architectures with stacking
- Reduced system level costs

Die Stacking



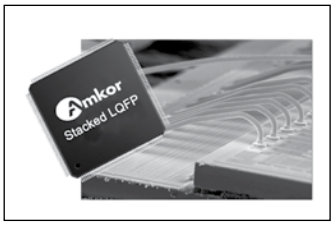


Amkor's die stacking technologies are widely deployed in high volume manufacturing across multiple factories and product lines. The key features: reliability, process and materials data are listed in the Stacked CSP data sheet. Customers rely on Amkor's turnkey and leading edge capabilities in design, assembly and test to solve their most complex 3D packaging or time to market challenges.

Next generation die stacking technology includes the ability to handle wafers and die thinned down to below 35 µm. It can then be reliably stacked and interconnected with up to 16 active devices high, employing leading edge die attach, wire bond and flip chip assembly capabilities.

Die stacking technologies have been demonstrated up to 24 high stacks, however, most stack ups greater than 9 devices high use a combination of die and package stacking technologies to address complex test, yield and logistic limitations.

Die stacking is also widely deployed in conventional leadframe-based packages including QFP, MLF® and SOP formats. Leveraging Amkor's industry leading infrastructure for high volume, low cost leadframe production, system designers can achieve significant savings in PCB real estate and overall cost.



Package Stacking (PoP – Package on Package)

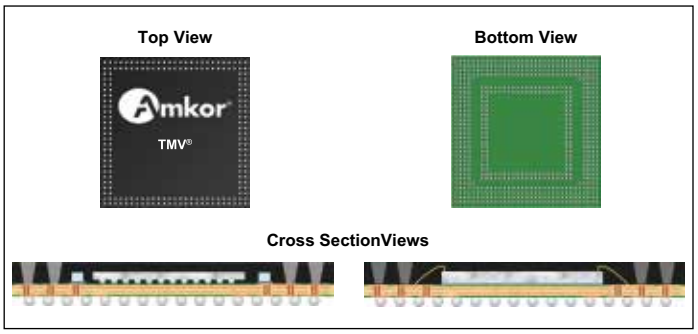
Stacking of fully assembled and tested packages is an area where Amkor has provided significant innovation to overcome the technical, business and logistics limitations associated with complex die stacks. Amkor launched the popular Package Stackable Very Thin Fine Pitch BGA (PSvfBGA) platform in 2004. PSvfBGA supports single die, stacked die using wirebond or hybrid (FC plus wirebond) stacks and has been applied to Flip Chip (FC) applications to improve warpage control and package integrity through test and SMT handling.

As handheld microprocessors have transitioned to advanced CMOS nodes with higher speed cores with higher I/O, there has been a transition from wirebond to flip chip die designs. Flip chip enables the use of an exposed die bottom package that integrates the package stacking design features of PSvfBGA in a fcCSP assembly flow, which Amkor calls Package Stackable Flip Chip Chip Scale Package (PSfcCSP). PSfcCSP has a thin exposed FC die enabling fine pitch stacked interfaces at 0.5 mm pitch which is a challenge in a center molded PSvfBGA structure.

Continued development resulted in Amkor entering the second generation of PoP applications where new memory architectures, required in mobile multimedia applications, demand higher density stacked interfaces in combination with PoP mounted area and height reductions. The previous PSvfBGA and PSfcCSP structures limited the ability of the memory interface to scale in density and pitch, resulting in the need for a new bottom PoP structure.

Amkor developed new technologies to create the next generation PoP solution with interconnect vias through the mold cap, naming this technology Through Mold Via (TMV®).TMV technology provides a stable bottom package that enables use of thinner substrates with a larger die to package ratio. TMV enabled PoP can support single, stacked die or FC designs. TMV is an ideal solution for the emerging 0.4 mm pitch low power DDR2 memory interface requirements and enables the stacked interface to scale with solder ball pitch densities to 0.3 mm pitch or below.

The next few years promise to provide many new challenges and applications for PoP, as handheld multimedia applications continue to demand higher signal processing power and data storage capabilities. Amkor is committed to maintaining strong development and production capabilities to ensure we are at the forefront in meeting next generation PoP requirements.



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